

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L5	1	"09/992120"	US-PGPUB; USPAT	OR	OFF	2006/03/24 10:27
L7	4	(US-6463582-\$ or US-5721927-\$ or US-5764962-\$ or US-6763452-\$). did.	USPAT	OR	OFF	2006/03/24 12:20
L8	5	US-4587612-\$.DID. OR US-4791558-\$.DID. OR US-5406644-\$.DID. OR US-5768593-\$.DID. OR US-6397242-\$.DID.	USPAT	OR	OFF	2006/03/24 12:33

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S82	25	S80 and (cisc with (risc powerpc))	US-PGPUB; USPAT	OR	OFF	2006/03/24 10:27
L5	1	"09/992120"	US-PGPUB; USPAT	OR	OFF	2006/03/24 10:27
S81	5	S80 and ("390" with (risc powerpc))	US-PGPUB; USPAT	OR	OFF	2006/03/23 19:07
S80	486	S78 and translst\$4	US-PGPUB; USPAT	OR	OFF	2006/03/23 19:06
S78	1565	(PSW or (Program adj status adj word))	US-PGPUB; USPAT	OR	OFF	2006/03/23 19:05
S74	10	S73 and (PSW or (Program adj status adj word))	USPAT	OR	OFF	2006/03/23 19:05
S73	50	("5560013").URPN.	USPAT	OR	OFF	2006/03/23 18:55
S72	50	("5560013").URPN.	USPAT	OR	OFF	2006/03/23 18:55
S71	2185	translation with mode	USPAT	OR	OFF	2006/03/23 17:13
S70	5	(dynamic adj object adj code adj translation)	USPAT	OR	OFF	2006/03/23 17:10
S69	0	(dynamic adj object adj code adj translation) with mode	USPAT	OR	OFF	2006/03/23 17:10
S68	11	(US-5560013-\$ or US-6142682-\$ or US-6516295-\$ or US-6704925-\$ or US-6163764-\$ or US-6530078-\$ or US-6457171-\$ or US-6091897-\$ or US-5678047-\$ or US-5150474-\$ or US-6415436-\$).did.	USPAT	OR	OFF	2005/07/10 14:26
S66	87	717/138.ccls.	USPAT	OR	OFF	2005/07/10 14:12
S65	4	"S/390" with legacy with instruction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/10 14:11
S64	380	(instruction with translst\$5 with (index flag table)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/10 14:11
S27	366	(instruction with translst\$5 with (index flag table)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/10 14:11

EAST Search History

S3	4	"S/390" with legacy with instruction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/10 14:11
S63	484	703/27.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/10 14:10
S62	317	(703/26).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/10 14:10
S61	1	"09/992120"	US-PGPUB; USPAT	OR	OFF	2005/07/10 12:39
S60	17	(US-20040194070-\$).did. or (US-4638423-\$ or US-5301302-\$ or US-5546552-\$ or US-5560013-\$ or US-5577233-\$ or US-5751982-\$ or US-5790825-\$ or US-5933622-\$ or US-6009261-\$ or US-6075937-\$ or US-6142682-\$ or US-6516295-\$ or US-6704925-\$ or US-6785801-\$ or US-6243668-\$ or US-5577231-\$).did.	US-PGPUB; USPAT	OR	OFF	2005/06/23 18:27
S59	2	(dynamic adj object adj code adj translation).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/23 13:52
S58	15	S57 and modifi\$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 21:09
S57	17	(US-20040194070-\$).did. or (US-4638423-\$ or US-5301302-\$ or US-5546552-\$ or US-5560013-\$ or US-5577233-\$ or US-5751982-\$ or US-5790825-\$ or US-5933622-\$ or US-6009261-\$ or US-6075937-\$ or US-6142682-\$ or US-6516295-\$ or US-6704925-\$ or US-6785801-\$ or US-6243668-\$ or US-5577231-\$).did.	US-PGPUB; USPAT	OR	OFF	2005/06/22 21:08

EAST Search History

S56	194	S55 and (TLB with (size index))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 20:32
S55	1206	(instruction with translation) and (TLB)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 20:32
S54	1	(instruction with translation) and (block adj tracking adj table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 20:32
S11	1	"09/992130"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 20:31
S53	17126	fujitsu.as.	USPAT	OR	OFF	2005/06/22 16:24
S52	190	amdahl.as.	USPAT	OR	OFF	2005/06/22 16:24
S51	7	(instruction with translat\$5) and hotspot	USPAT	OR	OFF	2005/06/22 16:18
S50	1	("6516295"),URPN.	USPAT	OR	OFF	2005/06/22 16:11
S49	23	legacy with instruction with translation	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 16:01
S48	110	translation adj index\$5	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 16:00
S47	61	S16 and (translation with (flag set indicator))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:58
S46	5	S16 and (translation with (done complet\$4) with (flag set indicator))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:50
S16	715	S7 or S9	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:48
S45	82	S44 and S41	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:44

EAST Search History

S44	581	(dynamic with translation) and index\$5	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:44
S43	25	S15 and S41	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:43
S15	206	instruction adj set adj simulat\$4	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:40
S42	172	((instruction with translation) and (index\$5 with (block table) with translation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:31
S41	1192	((instruction with translation) and (block with translation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:31
S37	2551	(instruction and (block with translation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:30
S40	119	S39 and index with table	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:24
S39	470	S38 and table	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:24
S38	545	S37 and emulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:24

EAST Search History

S7	317	(703/26).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 15:22
S28	214	(instruction with translat\$5 with (index flag table)) and (emulat\$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 14:26
S26	861	(instruction with translat\$5 with (index flag table set)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 14:03
S25	18148	(translat\$5 with (index flag table set)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:33
S21	190	S16 and flag	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:31
S23	1	S16 and (block with transform)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:27
S24	1	S23 and address	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:26
S19	63	S16 and (table with index)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:26
S22	11	S16 and translation with flag	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:13
S20	15	S16 and ((table with index) same translat\$5)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 13:13
S18	245	S17 and (translat\$5)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 12:24
S17	433	S16 and (table or index)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 12:24
S14	9	("4574344" "4635188" "4638423" "4761733" "5333287" "5406644" "5430862" "5481693" "5546552").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 11:45
S13	18	S12 and (store with instruction)	USPAT	OR	OFF	2005/06/22 10:30
S12	33	("4638423").URPN.	USPAT	OR	OFF	2005/06/22 10:29

EAST Search History

S8	82	S7 and (instruction with translat\$)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 10:22
S10	58	S9 and (instruction with translat\$)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 10:17
S9	484	703/27.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/22 10:17
S6	2	("5313614" "5404478").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/21 12:05
S5	19	"S/390" with emulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:05
S2	798	"S/390"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:05
S4	116	S2 and emulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:04
S1	165	legacy with instruction with (translat\$4 simulat\$4 execut\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:03



Search History (Beta)

Search History

- ☒ Web
- ☒ Images
- ☒ News
- ☒ Google
- ☐ Select all
- ☐ Pause
- ☐ Remove items
- ☐ Trends

Bookmarks ☆
Add bookmarks

Mar 24, 2006

No search history to show for this day

Mar 23, 2006 (cont.)

S390 "execution modes"

- ↳ S390 ELF Application Binary Interface Supplement - 5:45pm
www.linuxbase.org/spec/ELF/2Series/lsabio_s390.html
- ↳ S390 ELF Application Binary Interface Supplement - 5:43pm
www.busybox.net/_frunk/docs/psABI-s390.pdf?rev=10811

"dynamic object code translation"...what is

- ↳ Patent Search Results - 5:09pm
www.freepatentsonline.com/CCL717-138.html

"dynamic object code translation"...what is

- ↳ Method and apparatus for dynamic management of translated code... - 10:57am
www.freepatentsonline.com/6529862.html
- ↳ Reservoir Labs® - Advanced Compiler Development Services - 10:55am
www.reservoir.com/s/compiler.php

"dynamic object code translation"

- ↳ Reservoir Labs® - R-Stream Streaming Compiler - 10:55am
www.reservoir.com/r-dyn.php
- ↳ IBM Research: VLW - 10:52am
www.research.ibm.com/vlw/

Searches with no related results

S390 "execution modes" "legacy execution modes"

Mar 20, 2006

Network Processor Performance and Design Model with Benchmark Parameterization - Related history

- ↳ A Network Processor Performance and Design Model with Benchmark... - 2 weeks - 9:03am
www.ecs.umass.edu/ecw/pubs/2002/npw.html

Mar 19, 2006

"network processor"...resource utilization"

- ↳ PowerPoint Presentation - 8:03pm
www.cesr.ncsu.edu/ancs/sites/ANCS2005-04/yang.ppt

◀ Google

Previous 1 2 3 4 5 6 7 8 9 10 11 12 Next

Search Activity

Mar 2006

S	M	T	W	T	F	S
26	27	28	1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	1

Today, Mar 24

1-5 6-10 11-20 21+

Total searches: 228

Search History

Search the Web



Welcome United States Patent and Trademark Office

☐ Search Session History
[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Fri, 24 Mar 2006, 12:30:14 PM EST

Edit an existing query or
compose a new query in the
Search Query Display.

Search Query Display

Select a search number (#)
to:

- Add a query to the Search Query Display
- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Recent Search Queries

- #1 ((an eight issue tree-vliw processor for dynamic binary translation)<in>metadata)
- #2 (program status word<in>metadata)
- #3 (program status word<in>metadata)
- #4 ((psw<in>metadata) <and> (translation<in>metadata))<and> (cisc<in>metadata)
- #5 ((psw<in>metadata) <and> (translation<in>metadata))<and> (cisc<in>metadata)
- #6 (program status word<in>metadata)
- #7 (program status word<in>metadata)
- #8 ((an eight issue tree-vliw processor for dynamic binary translation)<in>metadata)
- #9 ((complete computer system simulation: the simos approach)<in>metadata)

Indexed by


[Help](#) [Contact Us](#) [Privacy & S](#)

© Copyright 2006 IEEE -



program status wc

Search

[Home](#) | [Products & services](#) | [Support & downloads](#) | [My account](#)

VLIW at IBM Research

Select a country

[← IBM Home](#)

IBM Research

[VLIW Home](#)[The VLIW project](#)[Basic Principles](#)[A VLIW based on tree instructions](#)[Processor Prototype](#)[VLIW Compiler](#)[Simulation Environment](#)[DAISY dynamic translation](#)

More information

[Talks and Presentations](#)[Publications and Patents](#)[Selected Abstracts](#)mikeg@watson.ibm.com

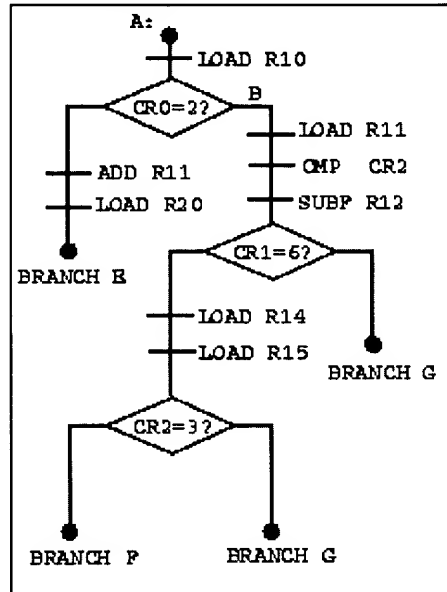
Introduction

The VLIW effort at the [IBM T.J. Watson Research Center](#) started in 1986, leading to our first publications [1, 2] describing a new approach to exploit instruction-level parallelism in branch-intensive programs. This approach is based on expressing a program as a sequence of [tree-instructions](#), each of which contains a multiway branch and multiple operations, all executable concurrently. Since then, three generations of a [parallelizing compiler](#) have been developed, a 8-unit VLIW processor prototype was designed and built, a [tree-based VLIW architecture](#) has been devised, a complete [simulation environment](#) has been developed, VLIW-based [techniques](#) have been introduced into existing compilers, and methods have been devised for [object code translation](#) from existing architectures into VLIW. Our recent work includes [open-source DAISY](#), a dynamic binary translation project aiming to represent legacy architectures as a layer of software on a VLIW, and [LaTTe](#), a joint Java (TM) JIT compiler project with Seoul National University, focusing on research into fast dynamic compilation techniques and instruction level parallelism in Java.

Our research activities include:

- The continuing development of compilation techniques to extract and exploit instruction-level parallelism (ILP) from programs.
- The development of architectures suited to use the ILP found through the compilation techniques.

Tree Instructions



Related Research

→ [DAISY](#)→ [LaTTe: an open-source JIT compiler](#)

More Information

→ [Talks and Presentations](#)→ [Publications and Patents](#)

- The continuing development of tools and an environment to simulate/evaluate the potential benefits of VLIW technology.
- The development of solutions to the limitations traditionally associated with VLIW architectures, such as
 - scalable implementations of VLIW;
 - static and dynamic object code translation for achieving binary compatibility;
 - software and hardware techniques for memory latency reduction.
- The integration of VLIW-based compilation techniques into existing compilers for IBM RS/6000 systems.

About IBM | Privacy | Legal | Contact

Update Inventor Search

Inventor Name Search Result

Page 1 of 2



PALM INTRANET

Day: Wednesday
Date: 3/22/2006
Time: 10:33:07

Inventor Name Search Result

Your Search was:

Last Name = HILTON
First Name = RONALD

Applicant#	Patent#	Status	Date Filed	Title	Inventor Name
09921120	Not Issued	71	11/14/2001	State-specific variants of translated code under emulation	HILTON, RONALD
09921121	Not Issued	71	11/14/2001	Flexible caching of translated code under emulation	HILTON, RONALD
09921130	Not Issued	71	11/14/2001	Processing of self-modifying code under emulation	HILTON, RONALD
09921137	Not Issued	90	11/14/2001	MEMORY ADDRESS PREDICTION UNDER EMULATION	HILTON, RONALD
08795305	38996339	150	02/07/1997	PLAIN CARBON STEEL SHUTTER FOR REMOVABLE DATA STORAGE CARTRIDGES	HILTON, RONALD A.
09201248	Not Issued	161	11/30/1998	DIGITAL PHONE SYSTEM	HILTON, RONALD D.
09201460	Not Issued	161	11/30/1998	METHOD AND APPARATUS FOR DYNAMIC DOMAIN NAMES	HILTON, RONALD D.
60067231	Not Issued	159	12/02/1997	METHOD AND APPARATUS FOR DYNAMIC DOMAIN NAMES	HILTON, RONALD D.
60067233	Not Issued	159	12/02/1997	DIGITAL PHONE SYSTEM	HILTON, RONALD D.
08796271	38996341	150	02/07/1997	PLAIN CARBON STEEL HUB FOR DATA STORAGE DEVICE	HILTON, RONALD L.
09211954	6292996	150	12/15/1998	METHOD OF MAKING A PLAIN CARBON STEEL HUB FOR DATA STORAGE DEVICE	HILTON, RONALD L.
11254290	Not Issued	30	10/19/2005	Processing of self-modifying code in multi-address-space and multi-processor systems	HILTON, RONALD N.
11254291	Not Issued	30	10/19/2005	Queue or stack based cache entry reclaim method	HILTON, RONALD N.
11221072	Not Issued	20	11/10/2005	Sparse cable compaction method	HILTON, RONALD N.
11221681	Not Issued	20	11/10/2005	Peer-based partitioning method for system resource sharing	HILTON, RONALD N.
11280554	Not Issued	20	11/15/2005	Distributed shared I/O cache subsystem	HILTON, RONALD N.
60620364	Not Issued	159	10/19/2004	Processing of self-modifying code in multi-address-space and multi-processor systems	HILTON, RONALD N.
60620365	Not Issued	159	10/19/2004	Queue or stack based cache entry reclaim method	HILTON, RONALD N.
60628332	Not Issued	159	11/15/2004	Distributed shared I/O cache subsystem	HILTON, RONALD N.
60628330	Not Issued	159	11/15/2004	Peer-based partitioning method for system resource	HILTON, RONALD N.
60628332	Not Issued	159	11/15/2004	Sparse cable compaction method	HILTON, RONALD N.
07816959	Not Issued	166	10/03/1992	S-UNIT ERROR HISTORY INHIBIT (EHI)	HILTON, RONALD N.

http://expoweb1-8002/cgi-bin/expo/InvInfo/invquery.pl?FAM_NAM=HILTON&GIV_NA... 3/24/2006

Inventor Name Search Result

Page 2 of 2

Issued	150	09/23/1992	FACILITY	HILTON, RONALD N.
07949583	5410668		RECONFIGURABLE CACHE MEMORY WHICH CAN SELECTIVELY INHIBIT ACCESS TO DAMAGED SEGMENTS IN THE CACHE MEMORY	
07950459	Not Issued	161	CONCURRENT BRANCH PROCESSING WITH DUAL INSTRUCTION DECODE	HILTON, RONALD N.
07954297	Not Issued	166	COMPUTER SYSTEM HAVING CACHE MEMORIES WITH INDEPENDENTLY VALIDATED KEYS IN THE TLB	HILTON, RONALD N.
07993082	5488706	150	A RETRY REQUEST SYSTEM IN A PIPELINE DATA PROCESSING SYSTEM WHERE EACH REQUESTING UNIT PRESERVES THE ORDER OF REQUESTS	HILTON, RONALD N.
08033415	Not Issued	161	S-UNIT ERROR HISTORY INHIBIT (EHI) FACILITY	HILTON, RONALD N.
08337133	5603008	150	COMPUTER SYSTEM HAVING CACHE MEMORIES WITH INDEPENDENTLY VALIDATED KEYS IN THE TLB	HILTON, RONALD N.

Inventor Search Completed: No Records to Display.

Last Name First Name
Search Another: Inventor HILTON RONALD Search

To go back use Back button on your browser toolbar.
Back to PALM ASSIGNMENT | OASIS | Home page

http://expoweb1-8002/cgi-bin/expo/InvInfo/invquery.pl?FAM_NAM=HILTON&GIV_NA... 3/24/2006



USPTO

Subscribe (Full Service) Register (Limited Service, Free) Login

Search: ☒ The ACM Digital Library ☐ The Guide

[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

THE ACM DIGITAL LIBRARY

Binary translation and architecture convergence issues for IBM system/390

Full text [PDF \(1.44 MB\)](#)

Source

International Conference on Supercomputing [archive](#)
Proceedings of the 14th international conference on Supercomputing [table of contents](#)
Santa Fe, New Mexico, United States
Pages: 338 - 347
Year of Publication: 2000
ISBN: 1-58113-270-0

Authors

Michael Gschwind IBM T.J. Watson Research Center, Yorktown Heights, NY
Kemal Ebcioglu IBM T.J. Watson Research Center, Yorktown Heights, NY
Erik Altman IBM T.J. Watson Research Center, Yorktown Heights, NY
Sumedh Sathaye IBM T.J. Watson Research Center, Yorktown Heights, NY

Sponsor SIGARCH: ACM Special Interest Group on Computer Architecture

Publisher ACM Press New York, NY, USA

Additional Information: [abstract](#) [references](#) [index terms](#) [collaborative colleagues](#) [peer to peer](#)

Tools and Actions:

[Discussions](#) [Find similar Articles](#) [Review this Article](#)
[Save this Article to a Binder](#) [Display Formats: BibTex EndNote ACM Ref](#)

DOI Bookmark:

Use this link to bookmark this Article: <http://doi.acm.org/10.1145/335231.335264>
[What is a DOI?](#)

↑ ABSTRACT

We describe the design issues in an implementation of the ESA/390 architecture based on binary translation to a very long instruction word (VLIW) processor. During binary translation, complex ESA/390 instructions are decomposed into instruction "primitives" which are then scheduled onto a wide-issue machine. The aim is to achieve high instruction level parallelism due to the increased scheduling and optimization opportunities which can be exploited by binary translation software, combined with the efficiency of long instruction word architectures. A further aim is to study the feasibility of a common execution platform for different instruction set architectures, such as ESA/390, RS/6000, AS/400 and the Java Virtual Machine, so that multiple systems can be built around a common execution platform.

↑ REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete list rather than only correct and linked references.

- 1 K. Ebcioglu and E. Altman. DAISY: dynamic compilation for 100% architectural compatibility. Research Report RC 20538, IBM T.J. Watson Research Center, Yorktown Heights, NY, 1996.
- 2 K. Ebcioglu, E. R. Altman, and E. Hokenek. A JAVA ILP machine based on fast dynamic

compilation. In IEEE MASCOTS International Workshop on Security and Efficiency Aspects of Java, January 1997.

3 J. E. Smith, T. Heil, S. Sastry, and T. M. Bezenek. Achieving high performance via co-designed virtual machines. In International Workshop on Innovative Architecture for Future Generation High-Performance Processors and Systems, pages 77-84, October 1998.

4 Gabriel M. Silberman, Kemal Ebcioglu. An architectural framework for migration from CISC to higher performance platforms. Proceedings of the 6th international conference on Supercomputing, p.198-215, July 19-24, 1992, Washington, D. C., United States

5 Gabriel M. Silberman, Kemal Ebcioglu. An Architectural Framework for Supporting Heterogeneous Instruction-Set Architectures. Computer, v.26 n.6, p.39-56, June 1993

6 Kemal Ebcioglu, Erik R. Altman. DAISY: dynamic compilation for 100% architectural compatibility. Proceedings of the 24th annual international symposium on Computer architecture, p.26-37, June 01-04, 1997, Denver, Colorado, United States

7 Kemal Ebcioglu, Erik R. Altman, Sumedh W. Sathaye, Michael Gschwind. Execution-Based Scheduling for VLIW Architectures. Proceedings of the 5th International Euro-Par Conference on Parallel Processing, p.1269-1280, August 31-September 03, 1999

8 Kemal Ebcioglu, Erik R. Altman, Michael Gschwind, Sumedh Sathaye. Optimizations and oracle parallelism with dynamic translation. Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture, p.284-295, November 16-18, 1999, Haifa, Israel

9 C. May. Mimic: a fast system/370 simulator. Papers of the Symposium on Interpreters and interpretive techniques, p.1-13, June 24-26, 1987, St. Paul, Minnesota, United States

10 S. Kim, S.-M. Moon, K. Ebcioglu, and E. Altman. VLIW: a Java just-in-time compiler for VLIW with fast scheduling and register allocation. To appear.

11 P. Hohensee, M. Myszewski, and D. Reese. WABI CPU emulation. In Hot Chips VIII, Palo Alto, CA, 1996.

12 M. Gschwind. Method for the deferred materialization of condition code information. Research Disclosures, 1999, (to appear).

13 K. Ebcioglu. Some design ideas for a VLIW architecture for sequential-natured software. In M. Cosnard et al., editor, Parallel Processing, pages 3-21. North-Holland, 1988. (Proceedings of IFIP WG 10.3 Working Conference on Parallel Processing).

14 Sarita V. Adve, Kourosh Gharachorloo. Shared Memory Consistency Models: A Tutorial, Computer, v.29 n.12, p.66-76, December 1996

15 J. Moreno and M. Moudgill. Method and apparatus for reordering of memory operations in a processor. US Patent No. 5,758,051, May 1998.

16 Eric L. Boyd, Edward S. Davidson. Hierarchical performance modeling with MACS: a case study of the convex C-240. Proceedings of the 20th annual international symposium on Computer architecture, p.203-210, May 16-19, 1993, San Diego, California, United States

17 Kemal Ebcioglu, Randy D. Groves, Ki-Chang Kim, Gabriel M. Silberman, Isaac Ziv. VLIW compilation techniques in a superscalar environment. Proceedings of the ACM SIGPLAN 1994 conference on Programming language design and implementation, p.36-48, June 20-24, 1994.

Cited References with this paper

Orlando, Florida, United States

18 Anton Chernoff, Mark Herdeg, Ray Hookway, Chris Reeve, Norman Rubin, Tony Tye, S. Bharadwaj Yadavalli, John Yates, FX132: A Profile-Directed Binary Translator, IEEE Micro, v.18 n.2, p.56-64, March 1998

19 Mendel Rosenblum, Stephen A. Herrod, Emmett Witchel, Anoop Gupta, Complete Computer System Simulation: The SimOS Approach, IEEE Parallel & Distributed Technology: Systems & Technology, v.3 n.4, p.34-43, December 1995

20 Richard L. Sites, Anton Chernoff, Matthew B. Kirk, Maurice P. Marks, Scott G. Robinson, Binary translation, Communications of the ACM, v.36 n.2, p.69-81, Feb. 1993

21 A. Klalber, The technology behind cruse processors. Technical report, Transmeta Corp., Santa Clara, CA, January 2000.

22 E. Kelly, R. Cmelik, and M. Wing, Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed. US Patent 5832205, November 1998.

23 Ravi Nair, Martin E. Hopkins, Exploiting instruction level parallelism in processors by caching scheduled groups, Proceedings of the 24th annual international symposium on Computer architecture, p.13-25, June 01-04, 1997, Denver, Colorado, United States

24 Eric Rotenberg, Quinn Jacobson, Yiannakis Sazeides, Jim Smith, Trace processors, Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture, p.138-148, December 01-03, 1997, Research Triangle Park, North Carolina, United States

25 An Eight Issue Tree-VLIW Processor for Dynamic Binary Translation, Proceedings of the International Conference on Computer Design, p.488, October 05-05, 1998

INDEX TERMS

Primary Classification:

- C. Computer Systems Organization
- ↳ C.5 COMPUTER SYSTEM IMPLEMENTATION
- ↳ C.5.1 Large and Medium ("Mainframe") Computers

↳ Nouns: IBM System/390

Additional Classification:

- C. Computer Systems Organization
- ↳ C.0 GENERAL
- ↳ Subjects: Instruction set design (e.g., RISC, CISC, VLIW)

General Terms:

Design, Measurement, Performance, Theory

Collaborative Colleagues:

Erik Altman: Yoo C. Chung Seungil Lee

<http://portal.acm.org/citation.cfm?id=335264&coll=ACM&dl=ACM&CFID=67925682&...> 3/24/2006

Kemal Ebcioglu Seungil Lee
 Kemal Ebcioglu Scott Mahke
 Kemal Ebcioglu Soo-Mook Moon
 Michael Jinpyo Park
 Gschwind Seongbae Park
 Suhyun Kim Sanjay Patel
 Heungbok Lee B. Ramakrishna Rau
 Je Hyung Lee Sumedh Sathaye
 Junpyo Lee Junpyo Lee
 Seungil Lee Byung-Sun Yang

Kemal Ebcioglu: Erik Altman
 Erik R. Altman
 Yoo C. Chung
 Michael Toshio Nakatani
 Gschwind Jinpyo Park
 Suhyun Kim Seongbae Park
 Heungbok Lee Dan Sahlin
 Je Hyung Lee Sumedh Sathaye
 Junpyo Lee Gabriel M. Silberman
 Seungil Lee Byung-Sun Yang

Michael
 Gschwind:

Kemal Ebcioglu
 Alexandre E. Eichenberger
 Philip G. Emma
 Alan Gara
 Mark Giampapa
 Manish Gupta
 Blumrich Shawn Hall
 Pradipt Bose Ruud A. Haring
 Arthur A. Bright Philip Heidelberg
 David Brooks Dong Chen
 Tong Chen Dirk Hoenicke
 Paul Coteus Gerard V. Kopsay
 Kemal Ebcioglu Paul Ledak
 Erik Altman
 Erik R. Altman
 David
 Appenzeller
 Thomas M. Conte
 Kemal Ebcioglu
 Michael Gschwind
 Paul Ledak
 Sumedh
 Sathaye:
 Oliver
 Malschberger
 Dietmar Maurer
 Christian Maunder
 Kathryn O'Brien
 Kevin O'Brien
 Peter H. Oden
 Martin Ohmacht
 Daniel A. Prener
 Rick A. Rand
 Valentina Salapura
 Tao Zhang
 Sumedh Sathaye
 Sumedh W. Sathaye
 Victor Zyuban
 Janice C. Shepherd
 Byoungro So
 Vili Srinivasan
 Philip N. Strenski
 Zehra Sura
 Todd Takken
 Pavlos Vranas
 Amy Wang
 Peng Wu
 Peng Zhao





Peer to Peer - Readers of this Article have also read:

- Data structures for quadtree approximation and compression
- Communications of the ACM** 28, 9
- Hanan Samet
- A hierarchical single-key-lock access control using the Chinese remainder theorem
- Proceedings of the 1992 ACM/SIGAPP Symposium on Applied computing**
- Kim S. Lee, Huizhu Lu, D. D. Fisher

<http://portal.acm.org/citation.cfm?id=335264&coll=ACM&dl=ACM&CFID=67925682&...> 3/24/2006

- The GemStone object database management system
Communications of the ACM 34, 10
Paul Butterworth, Allen Otis, Jacob Stein
- Putting innovation to work: adoption strategies for multimedia communication systems
Communications of the ACM 34, 12
Ellen Franck, Susan Ehrlich Rudman, Donna Cooper, Stephen Levine
- An intelligent component database for behavioral synthesis
Proceedings of the 27th ACM/IEEE conference on Design automation
Gwo-Dong Chen, Daniel D. Gajski

The ACM Portal is published by the Association for Computing Machinery. Copyright © 2006 ACM, Inc.
[Terms of Usage](#) [Privacy Policy](#) [Code of Ethics](#) [Contact Us](#)

Useful downloads:  Adobe Acrobat  QuickTime  Windows Media Player  Real Player